Quality Information

VISHAY SEMICONDUCTORS' CONTINUOUS IMPROVEMENT

- Quality training for ALL personnel including production, development, marketing and sales departments
- Zero defect mindset
- Permanent quality improvement process
- Total Quality Management (TQM)
- Vishay Semiconductors' Quality Policy established by the management board
- Quality system certified per ISO 9001 2008
- Quality system certified per ISO/TS 16949:2009
- Environmental system certified per ISO 14001:2004

VISHAY SEMICONDUCTORS' TOOLS FOR CONTINUOUS IMPROVEMENT

- Vishay Semiconductors follows the rules of the EFQM - Quality - Management system
- Vishay Semiconductors qualifies materials, processes and process changes
- Vishay Semiconductors uses process FMEA (failure mode and effects analysis) for all processes. Process and machine capability as well as Gauge R & R (Repeatability & Reproducibility) are proven
- Vishay Semiconductors' internal qualifications correspond to IEC 68-2 and MIL-STD 883 and AEC-Q101
- Vishay Semiconductors periodically requalifies device types (long term monitoring)
- Vishay Semiconductors uses SPC for significant production parameters. SPC is performed by trained operators
- Vishay Semiconductors' 2 x 100 % testing of final products
- Vishay Semiconductors' lot release is carried out via sampling. Sampling acceptance criterion is always c = 0

Fig. 1

VISHAY.

CREATE FIRST-CLASS QUALITY, ON-TIME DELIVERY, AND SATISFY CUSTOMERS' REQUIREMENTS

ZERTIFIKAT ◆ CERTIFICATE ◆ 認証証書 ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

TÜV SÜD Management Service

CERTIFICATE

The Certification Body
of TÜV SÜD Management Service GmbH
certifies that

VISHAY Semiconductor Ges.m.b.H
Telefunkenstrasse 5, A-4840 Vöcklabruck / AUSTRIA

has established and applies
a Quality Management System for

Design, Manufacture and Sales of Small Signal Products

An audit was performed, Report No. **70004203**
Proof has been furnished that the requirements according to

ISO 9001:2008

are fulfilled. The certificate is valid until **2012-08-24**
Certificate Registration No. **12 100 12741 TMS**

Munich, 2009-09-15

QMS-TGA-ZM-07-92

Page 1 of 1

TÜV SÜD Management Service GmbH • Zertifizierstelle • Ridlerstraße 65 • 80339 München • Germany

Fig. 2 - Vishay Semiconductor, A-Voecklabruck, ISO 9001:2008

Within a certification audit, the
Vishay Semiconductor (Austria) Ges.m.b.H

at the location A-4840 Vöcklabruck, Telefunkenstraße 5 has proven that, meeting the requirements of the international standard EN ISO 14001, an environmental policy was published, an environmental management system is maintained and management system audits are performed regularly.

Certificate

No. u-12402-3

of an
Environmental Management System
according to

Berlin, June 12th 2007

ISO 14001
Issued November 2004

For the Business Activities:
Development and manufacture of electronic devices

This certificate is held since 1998 and is valid until June 12th 2010.

Dr.-Ing. Jan Uwe Lieback
Environmental verifier DE-V-0026

Dipl.-Ing. Dirk Horstmann
Environmental verifier DE-V-0262

Dipl.-Phys. Andreas Lemke
Certification office

GUT

DAU DE-V-0213

Fig. 4 - Vishay Semiconductor, A-Voecklabruck, ISO 14001

ZERTIFIKAT ◆ CERTIFICATE ◆ 認証証書 ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

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VISHAY Semiconductor Ges.m.b.H
Telefunkenstrasse 5, A-4840 Vöcklabruck / AUSTRIA

has established and applies
a Quality Management System for

Design and Manufacture of Small Signal Products
(with Product Design as per Chapter 7.3)

An audit was performed, Report No. **70004203**
Proof has been furnished that the requirements according to

ISO/TS 16949:2009
Third Edition 2009-06-15

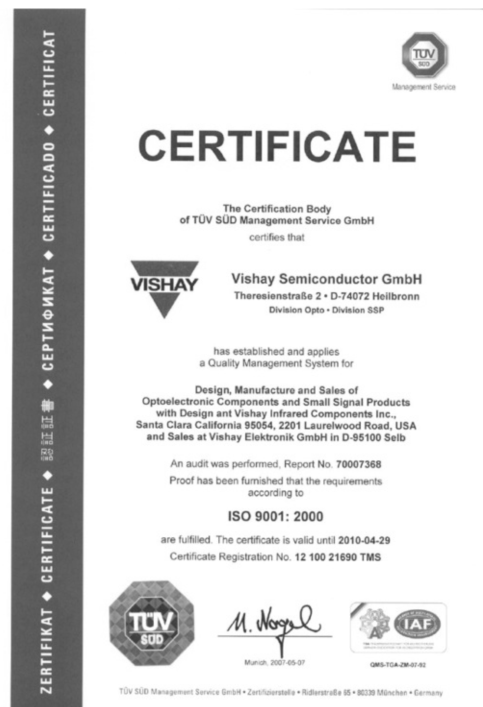
are fulfilled. The certificate is valid from **2009-08-25** until **2012-08-24**
Certificate Registration No.: **12 111 12741 TMS**
IATF Certificate No.: **0087574**

Munich, 2009-09-15

Page 1 of 1

TÜV SÜD Management Service GmbH • Zertifizierstelle • Ridlerstraße 65 • 80339 München • Germany

Fig. 3 - Vishay Semiconductor, A-Voecklabruck, ISO/TS 16949:2009



ZERTIFIKAT ◆ CERTIFICATE ◆ 認証証書 ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

TÜV SÜD Management Service

CERTIFICATE

The Certification Body
of TÜV SÜD Management Service GmbH
certifies that

Vishay Semiconductor GmbH
Theresienstraße 2 • D-74072 Heilbronn
Division Opto • Division SSP

has established and applies
a Quality Management System for

Design, Manufacture and Sales of Optoelectronic Components and Small Signal Products with Design ant Vishay Infrared Components Inc., Santa Clara California 95054, 2201 Laurelwood Road, USA and Sales at Vishay Elektronik GmbH in D-95100 Selb

An audit was performed, Report No. **70007368**
Proof has been furnished that the requirements according to

ISO 9001: 2000

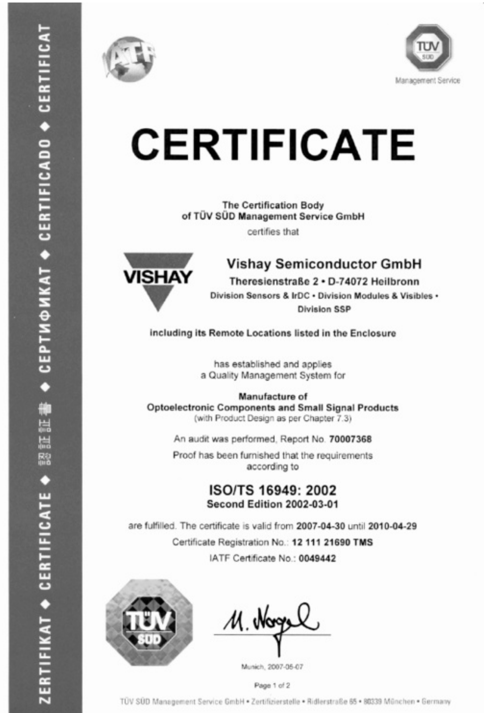
are fulfilled. The certificate is valid until **2010-04-29**
Certificate Registration No. **12 100 21690 TMS**

Munich, 2007-05-07

QMS-TGA-ZM-07-92

TÜV SÜD Management Service GmbH • Zertifizierstelle • Ridlerstraße 65 • 80339 München • Germany

Fig. 5 - Vishay Semiconductor, D-Heilbronn, ISO 9001:2000



ZERTIFIKAT ◆ CERTIFICATE ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

Management Service

CERTIFICATE

The Certification Body
of TÜV SÜD Management Service GmbH
certifies that

Vishay Semiconductor GmbH
Theresienstraße 2 • D-74072 Heilbronn
Division Sensors & IrDC • Division Modules & Visibles • Division SSP

including its Remote Locations listed in the Enclosure

has established and applies
a Quality Management System for

**Manufacture of
Optoelectronic Components and Small Signal Products**
(with Product Design as per Chapter 7.3)

An audit was performed, Report No. 70007368
Proof has been furnished that the requirements
according to

ISO/TS 16949: 2002
Second Edition 2002-03-01

are fulfilled. The certificate is valid from 2007-04-30 until 2010-04-29
Certificate Registration No.: 12 111 21690 TMS
IATF Certificate No.: 0049442

Munich, 2007-06-07

Page 1 of 2

TÜV SÜD Management Service GmbH • Zertifizierstelle • Ridlerstraße 65 • 80339 München • Germany

Fig. 6 - Vishay Semiconductor, D-Heilbronn,
ISO/TS 16949:2002

Certificate

Standard: **ISO 9001:2008**

Certificate Registr. No.: 01 100 99463

TÜV Rheinland Cert GmbH certifies:

Certificate Holder: **Vishay Semiconductor Shanghai Co., Ltd.**
501 West Jiang Chang Road,
Shanghai 200436, P. R. China

Scope: Design and Manufacturing of Diodes, Transistors

An audit was performed, Report No. 99463. Proof has been furnished that the requirements according to ISO 9001:2008 are fulfilled.
The due date for all future audits is 02-06 (dd.mm).

Validity: The certificate is valid from 2009-07-17 until 2012-07-16.
First certification 2004

Hong Kong, 2009-07-17

TÜV Rheinland Cert GmbH *)
Am Grauen Stein · 51105 Köln

TGA-ZM-58-95-00

www.tuv.com

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Precisely Right.

Fig. 8 - Vishay Semiconductor Shanghai,
ISO 9001:2008

ZERTIFIKAT ◆ CERTIFICATE ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

Management Service

CERTIFICATE

The Certification Body
of TÜV SÜD Management Service GmbH
certifies that

Vishay Semiconductor GmbH
Theresienstraße 2
D-74072 Heilbronn

has established and applies
an Environmental Management System for

**Design, Manufacture and Sales
of Optoelectronic Components
and Small Signal Products.**

An audit was performed, Report No. 70007368
Proof has been furnished that the requirements
according to

ISO 14001: 2004

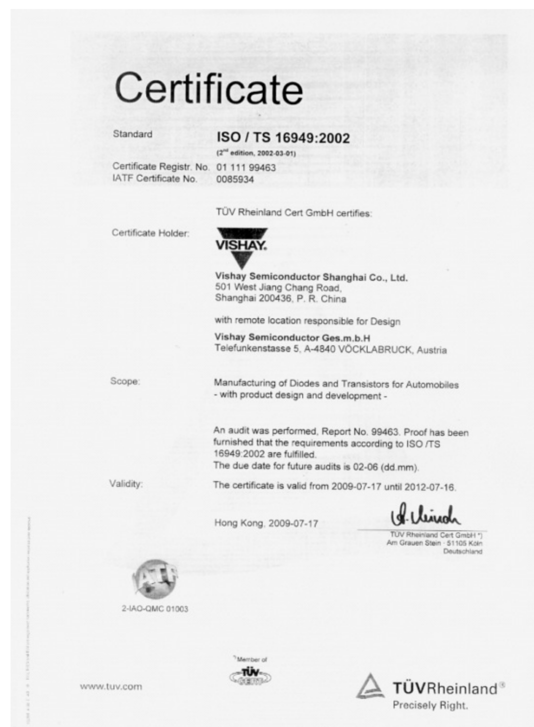
are fulfilled. The certificate is valid until 2011-02-11
Certificate Registration No. 12 104 21690 TMS

Munich, 2008-02-14

EMS-TGA-ZM-07-92

TÜV SÜD Management Service GmbH • Zertifizierstelle • Ridlerstraße 65 • 80339 München • Germany

Fig. 7 - Vishay Semiconductor, D-Heilbronn,
ISO 14001:2004



Certificate

Standard: **ISO / TS 16949:2002**
(2nd edition, 2002-03-01)

Certificate Registr. No.: 01 111 99463
IATF Certificate No.: 0085934

TÜV Rheinland Cert GmbH certifies:

Certificate Holder: **Vishay Semiconductor Shanghai Co., Ltd.**
501 West Jiang Chang Road,
Shanghai 200436, P. R. China

with remote location responsible for Design
Vishay Semiconductor Ges.m.b.H
Telefunkenstasse 5, A-4840 VÖCKLABRUCK, Austria

Scope: Manufacturing of Diodes and Transistors for Automobiles
- with product design and development -

An audit was performed, Report No. 99463. Proof has been furnished that the requirements according to ISO /TS 16949:2002 are fulfilled.
The due date for future audits is 02-06 (dd.mm).

Validity: The certificate is valid from 2009-07-17 until 2012-07-16.

Hong Kong, 2009-07-17

TÜV Rheinland Cert GmbH *)
Am Grauen Stein · 51105 Köln
Deutschland

2-IAO-QMC 01003

www.tuv.com

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Precisely Right.

Fig. 9 - Vishay Semiconductor Shanghai,
ISO/TS 16949:2002

Certificate

Standard ISO 14001:2004

Certificate Registr. No. 01 104 000495

TÜV Rheinland Cert GmbH certifies:

Certificate Holder: VISHAY

Vishay Semiconductor Shanghai Co., Ltd.
501 West Jiang Chang Road,
Shanghai 200436, P. R. China

Scope: Manufacturing of Diodes and Transistors

An audit was performed, Report No. 000495. Proof has been furnished that the requirements according to ISO 14001:2004 are fulfilled.
The due date for all future audits is 25-10 (dd.mm).

Validity: The certificate is valid from 2009-11-29 until 2013-01-10.
First certification 2001

Hong Kong, 2009-11-29

TÜV Rheinland Cert GmbH *)
Am Grauen Stein · 51105 Köln

TGA-ZM-58-95-60

*) Member of TÜV CERT

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Fig. 10 - Vishay Semiconductor Shanghai,
ISO 14001:2004

EUROCERT

Certificate of Approval

Based on it's procedure
EUROCERT Qualifying and Certifying Ltd. certifies, that

VISHAY HUNGARY Ltd.,
Budapest, Hungary.

has implemented and operates an environmental management system,
which complies with the

ISO 14001: 2004

standard.

Scope of acrivity/service: Production of microelectronic devices and systems.

Sites: 1047 Budapest, Fóti út 56.

This certificate is valid 13. 05. 2011.

Certificate registration number: KMR 035

Budapest, 13th of May, 2008

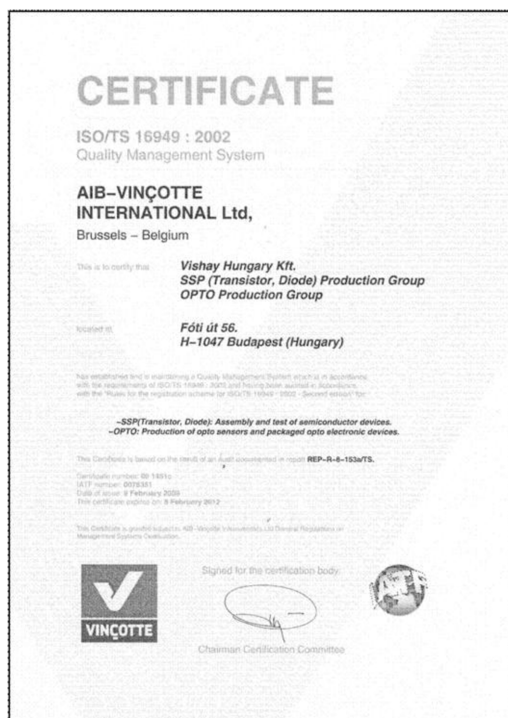
ISO 14001: 2004 EUROCERT

IAF

SNAS
Reg.No. 187/R-026

Péter Oláh
managing director

Fig. 12 - Vishay Semiconductor Hungary,
ISO 14001:2004



CERTIFICATE

ISO/TS 16949 : 2002
Quality Management System

AIB–VINÇOTTE
INTERNATIONAL Ltd,
Brussels – Belgium

This is to certify that *Vishay Hungary Kft.*
SSP (Transistor, Diode) Production Group
OPTO Production Group

located at *Fóti út 56.*
H–1047 Budapest (Hungary)

–SSP(Transistor, Diode): Assembly and test of semiconductor devices.
–OPTO: Production of opto sensors and packaged opto electronic devices.

VINÇOTTE

Signed for the certification body

Chairman Certification Committee

Fig. 11 - Vishay Semiconductor Hungary,
ISO/TS 16949:2002

GENERAL QUALITY FLOW CHART

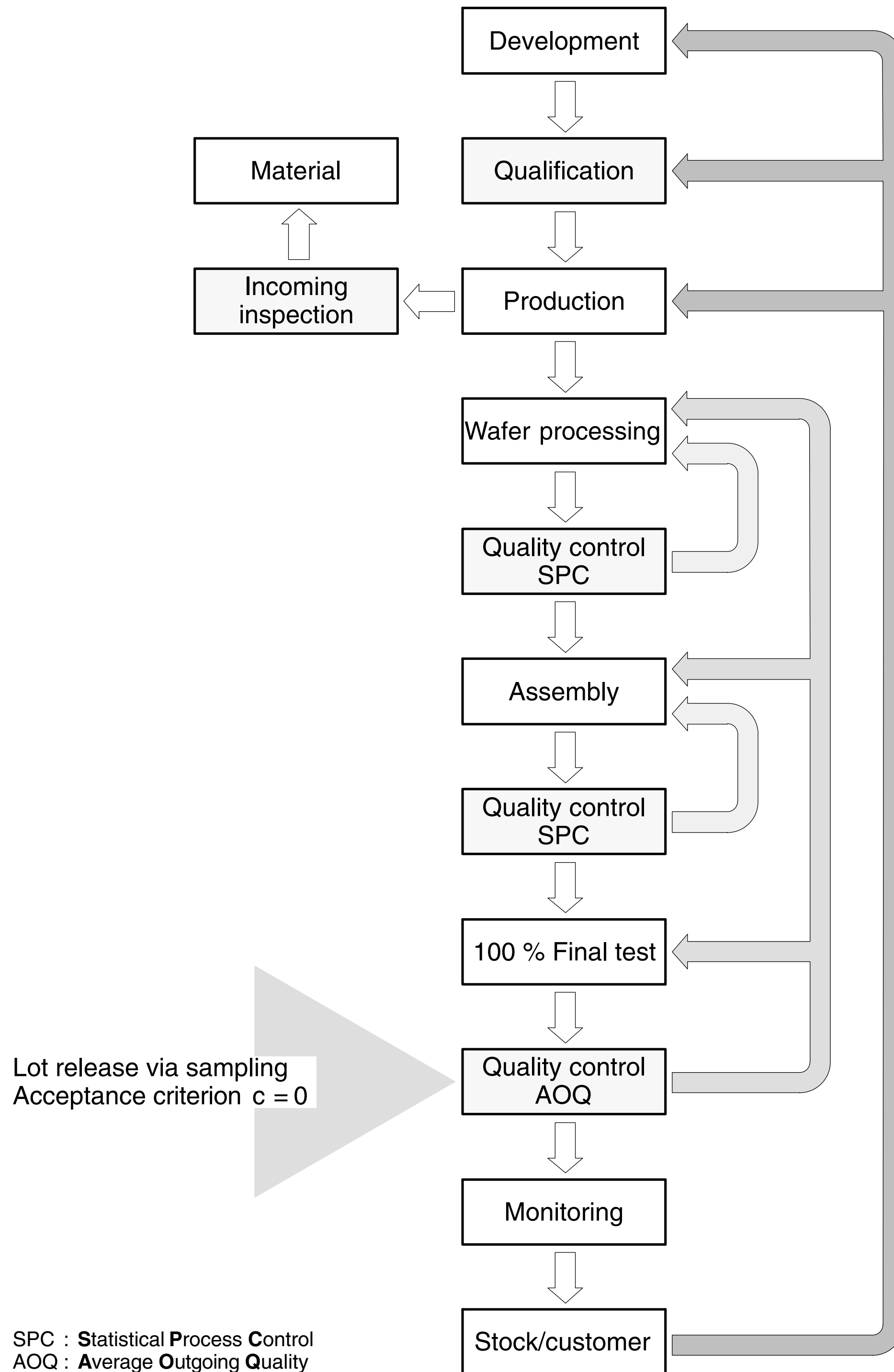


Fig. 13

VISHAY QUALITY ROAD MAP

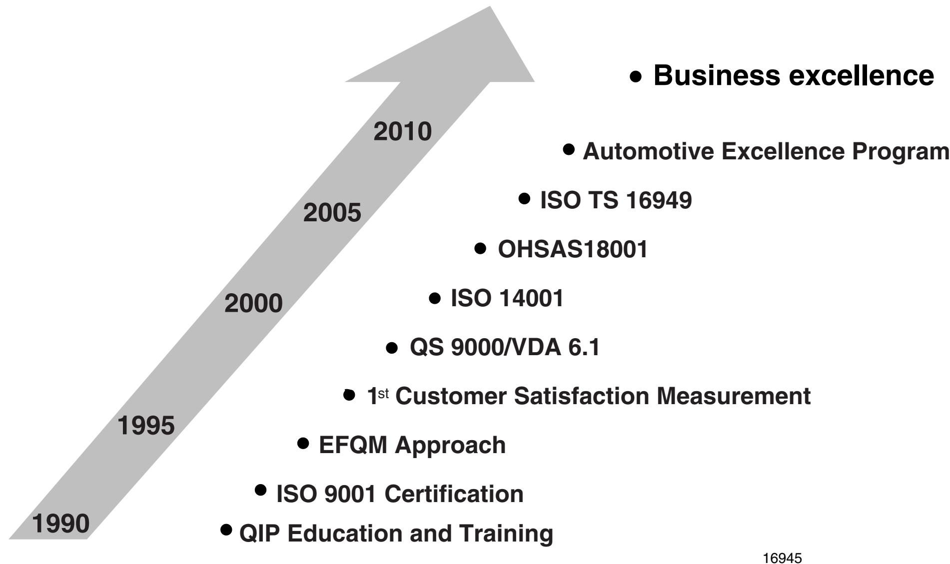


Fig. 14

QUALIFICATION AND RELEASE

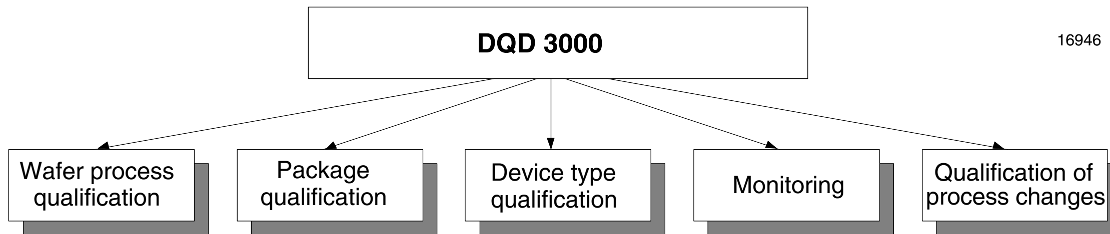


Fig. 15

New wafer processes, packages and device types are qualified according to the internal Vishay Semiconductors specification DQD 3000.
DQD 3000 consists of five parts (see figure 18.).

Wafer process release

The wafer process release is the fundamental release qualification for the various technologies used by Vishay Semiconductors. Leading device types are defined for various technologies. Three wafer lots of these types are subjected to an extensive qualification procedure and are used to represent this technology. A positive result will lead to release of the technology.

Package release:

The package release is the fundamental release qualification for the different packages used. Package groups are defined.
Critical packages are selected: two assembly lots are subjected to the qualification procedure represented. A positive result will release all similar packages.

Device type release

The device type released is the release of individual designs.

Monitoring

Monitoring serves both as the continuous monitoring of the production and as a source of data for calculation of early failures (early failure rate: EFR).

Product or process changes are released via ECN (Engineering Change Note). This includes proving process capability and meeting the quality requirements.
Test procedures utilized are IEC 68-2-... and MIL-STD-750 respectively.

STATISTICAL METHODS FOR PREVENTION

To manufacture high-quality products, it is not sufficient to inspect the product at the end of the production process.
Quality has to be “designed-in” during process and product development. In addition to that, the “designing-in” must also be ensured during production flow. Both will be achieved by means of appropriate measurements and tools.

- Statistical Process Control (SPC)
- R & R- (Repeatability and Reproducibility) tests
- Up-Time Control (UTC)
- Failure Mode and Effect Analysis (FMEA)
- Design Of Experiments (DOE)
- Quality Function Deployment (QFD)

Vishay has been using SPC as a tool in production since 1990/91.
By using SPC, deviations from the process control goals are quickly established. This allows control of the processes before the process parameters run out of specified limits. To assure control of the processes, each process step is observed and supervised by trained personnel. Results are documented.
Process capabilities are measured and expressed by the process capability index (C_{pk}).
Validation of the process capability is required for new processes before they are released for production.
Before using new equipment and new gauges in production, machine capability (C_{mk} = machine capability index) or R & R (Repeatability & Reproducibility) is used to validate the equipment's fitness for use.
Up-Time is recorded by an Up-Time Control (UTC) system. This data determines the intervals for preventive maintenance, which is the basis for the maintenance plan.
A process-FMEA is performed for all processes (FMEA = Failure Mode and Effect Analysis). In addition, a design- or product-FMEA is used for critical products or to meet agreed customer requirements.
Design of Experiments (DOE) is a tool for the statistical design of experiments and is used for optimization of processes. Systems (processes, products and procedures) are analyzed and optimized by using designed experiments.
A significant advantage compared to conventional methods is the efficient performance of experiments with minimum effort by determining the most important inputs for optimizing the system.
As a part of the continuous improvement process, all Vishay employees are trained in TQM thinking and in using new statistical methods and procedures.

RELIABILITY

The requirements concerning quality and reliability of products are always increasing. It is not sufficient to only deliver fault-free parts. In addition, it must be ensured that the delivered goods serve their purpose safely and failure of free, i.e. reliably. From the delivery of the device and up to its use in a final product, there are some occasions where the device or the final product may fail despite testing and outgoing inspection.
In principle, this sequence is valid for all components of a product.
For these reasons, the negative consequences of a failure, which become more serious and expensive the later they occur, are obvious. The manufacturer is therefore interested in supplying products with the lowest possible

- AOQ (Average Outgoing Quality) value
- EFR (Early Failure Rate) value
- LFR (Long-term Failure Rate) value

AVERAGE OUTGOING QUALITY (AOQ)

All outgoing products are sampled after 2 x 100 % testing. This is known as "Average Outgoing Quality" (AOQ). The results of this inspection are recorded in ppm (parts per million) using the method defined in JEDEC 16.

EARLY FAILURE RATE (EFR)

EFR is an estimate (in ppm) of the number of early failures related to the number of devices used. Early failures are normally those which occur within the first 300 h to 1000 h. Essentially, this period of time covers the guarantee period of the finished unit.
Low EFR values are therefore very important to the device user. The early life failure rate is heavily influenced by complexity. Consequently, “designing-in” of better quality during the development and design phase, as well as optimized process control during manufacturing, significantly reduces the EFR value. Normally, the early failure rate should not be significantly higher than the random failure rate. EFR is given in ppm (parts per million).

LONG-TERM FAILURE RATE (LFR)

LFR shows the failure rate during the operational period of the devices. This period is of particular interest to the manufacturer of the final product. Based on the LFR value, estimations concerning long-term failure rate, reliability and a device's or module's operational life may be derived. The usage life time is normally the period of constant failure rate. All failures occuring during this period are random.
Within this period the failure rate is:

$$\lambda = \frac{\text{Sum of failures}}{\Sigma\ (\text{Quantity} \times \text{Time to failure})} \times \frac{1}{\text{h}}$$

The measure of λ is FIT (Failures In Time = number of failures in 10^9 device hours).

Example

A sample of 500 semiconductor devices is tested in a operating life test (dynamic electric operation). The devices operate for a period of 10 000 h.

Failures:

1 failure after 1000 h

1 failure after 2000 h

The failure rate may be calculated from this sample by

$$\lambda = \frac{2}{1 \text{ x } 1000 + 1 \text{ x } 2000 + 498 \text{ x } 10\,000} \times \frac{1}{h}$$

$$\lambda = \frac{2}{4\,983\,000} \times \frac{1}{h} = 4.01 \times 10^{-7} \frac{1}{h}$$

This is a λ-value of 400 FIT, or this sample has a failure rate of 0.04 %/1000 h on average.

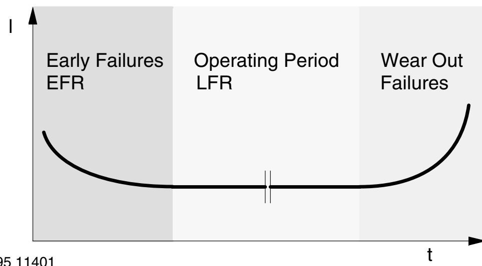


Fig. 16 - Bath Tub Curve

CONFIDENCE LEVEL

The failure rate λ calculated from the sample is an estimate of the unknown failure rate of the lot.

The interval of the failure rate (confidence interval) may be calculated, depending on the confidence level and sample size.

The following is valid:

- The larger the sample size, the narrower the confidence interval.
- The lower the confidence level of the statement, the narrower the confidence interval.

The confidence level applicable to the failure rate of the whole lot when using the estimated value of λ is derived from the x^2-distribution. In practice, only the upper limit of the confidence interval (the maximum average failure rate) is used.

Therefore:

$$\lambda_{max.} = \frac{x^2/2(r;P_A)}{n \times t} \text{ in } \frac{1}{h}$$

$$LFR = \frac{x^2/2(r;P_A)}{n \times t} \times 1 \times 10^9 \text{ in (FIT)}$$

r: Number of failures

PA: Confidence level

n: Sample size

t: Time in hours

n x t: Device hours

The $x^2/2$ for λ are taken from table 1.

For the above example from table 1:

$x^2/2$ (r = 2; PA = 60 %) = 3.08

n x t = 4 983 000 h

$$\lambda = \frac{3.08}{4\,983\,000} = 6.8 \times 10^{-7} \frac{1}{h}$$

This means that the failure rate of the lot does not exceed 0.0618 %/1000 h (618 FIT) with a probability of 60 %.

If a confidence level of 90 % is chosen from table 1:

$x^2/2$ (r = 2; PA = 90 %) = 5.3

$$\lambda_{max.} = \frac{5.3}{4\,983\,000} = 1.06 \times 10^{-6} \frac{1}{h}$$

This means that the failure rate of the lot does not exceed 0.106 %/1000 h (1060 FIT) with a probability of 90 %.

TABLE 1

NUMBER OF FAILURES	CONFIDENCE LEVEL			
	50 %	60 %	90 %	95 %
0	0.60	0.93	2.31	2.96
1	1.68	2.00	3.89	4.67
2	2.67	3.08	5.30	6.21
3	3.67	4.17	6.70	7.69
4	4.67	5.24	8.00	9.90
5	5.67	6.25	9.25	10.42
6	6.67	7.27	10.55	11.76
7	7.67	8.33	11.75	13.16
8	8.67	9.35	13.00	14.30
9	9.67	10.42	14.20	15.63
10	10.67	11.42	15.40	16.95

OPERATING LIFE TESTS

Number of devices tested: $n = 50$
Number of failures:
(positive qualification): $c = 0$
Test time: $t = 2000$ h
Confidence level: PA = 60 %
$x^2/2$ (0; 60 %) = 0.93

$$\lambda_{max.} = \frac{0.93}{50 \times 2000} = 9.3 \times 10^{-6}\ \frac{1}{h}$$

This means, that the failure rate of the lot does not exceed 0.9 %/1000 h (9300 FIT) with a probability of 60 %.
This example demonstrates that it is only possible to verify LFR values of 9300 FIT with a confidence level of 60 % in a normal qualification test (50 devices, 2000 h).
To obtain LFR values which meet today's requirements (< 50 FIT), the following conditions have to be fulfilled:

- Very long test periods
- Large quantities of devices
- Accelerated testing (e.g. higher temperature)

MEAN TIME TO FAILURE (MTTF)

For systems which can not be repaired and whose devices must be changed, e.g. semiconductors, the following is valid:

$$MTTF = \frac{1}{\lambda}$$

MTTF is the average fault-free operating period per a monitored (time) unit.

ACCELERATING STRESS TESTS

Innovation cycles in the field of semiconductors are becoming shorter and shorter. This means that products must be brought to the market quicker. At the same time, expectations concerning the quality and reliability of the products have become higher.
Manufacturers of semiconductors must therefore assure long operating periods with high reliability but in a short time. Sample stress testing is the most commonly used way of assuring this.
The rule of Arrhenius describes this temperature dependent change of the failure rate.

$$\lambda (T_2) = \lambda (T_1) \times e^{\left[\frac{E_A}{k} \times \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]}$$

Boltzmann's constant
$k = 8.63 \times 10^{-5}$ eV/K
Activation energy
E_A in eV
Junction temperature real operation
T_1 in Kelvin
Junction temperature stress test
T_2 in Kelvin
Failure rate real operation
$\lambda (T_1)$
Failure rate stress test
$\lambda (T_2)$
The acceleration factor is described by the exponential function as being:

$$AF = \frac{\lambda (T_2)}{\lambda (T_1)} = e^{\left[\frac{E_A}{k} \times \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]}$$

Example

The following conditions apply to an operating life stress test:
Environmental temperature during stress test
$T_A = 70$ °C
Power dissipation of the device
$P_V = 100$ mW
Thermal resistance junction/environment
$R_{thJA} = 300$ K/W
The system temperature/junction temperature results from:
$T_J = T_A + R_{thJA} \times P_V$
$T_J = 70$ °C + 300 K/W 100 mW
$T_J = 100$ °C
Operation in the field at an ambient temperature of 50 °C and at an average power dissipation of 80 mW is utilized. This results in a junction temperature in operation of $T_J = 74$ °C. The activation energy used for opto components is $E_A = 0.8$ eV.
The resulting acceleration factor is:

$$AF = \frac{\lambda (373\ K)}{\lambda (347\ K)} = e^{\left[\frac{E_A}{k} \times \left(\frac{1}{347\ K} - \frac{1}{373\ K}\right)\right]}$$

$AF \approx 6.5$

This signifies that, in this example, the failure rate is lower by a factor of 6.5 compared to the stress test.
Other accelerating stress tests may be:

- Humidity (except displays type TDS.)
  $T_A = 85$ °C
  RH = 85 %
- Temperature cycling
  Temperature interval as specified

The tests are carried out according to the requirements of appropriate IEC-standards (see also chapter “Qualification and Release”).

ACTIVATION ENERGY

There are some conditions which need to be fulfilled in order to use Arrhenius' method:

- The validity of Arrhenius' rule has to be verified
- "Failure-specific" activation energies must be determined

These conditions may be verified by a series of tests. Today, this procedure is generally accepted and used as a basis for estimating operating life. The values of activation energies can be determined by experiments for different failure mechanisms.
Values often used for different device groups are:

Opto components	0.8 eV
Bipolar ICs	0.7 eV
MOS ICs	0.6 eV
Transistors	0.7 eV
Diodes	0.7 eV
Sinterglass Diodes	0.7 eV

By using this method, it is possible to provide longterm predictions for the actual operation of semiconductors even with relatively short test periods.

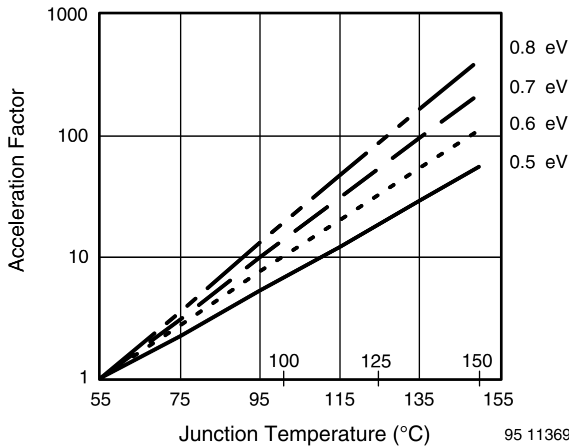


Fig. 17 - Acceleration Factor for Different Activation Energies Normalized to T_J = 55 °C